SiT5711 ADVANCED

1 to 60 MHz Emerald Platform™ Stratum 3E Oscillator

Description

The SiT5711 is the industry's smallest (9 mm x 7 mm) package, stratum 3E compliant oscillator with ±5 ppb over-temp stability and ±0.8 ppb per day short term aging.

By combining SiTime's unique DualMEMS™ temperature sensing and TurboCompensation™ technology, the SiT5711 delivers stable timing in the presence of environmental hazards – air flow, temperature perturbation, vibration, shock and electromagnetic interference (EMI). This environmental robustness enables placement of the device anywhere on the PCB without any cover or mechanical shielding.

The SiT5711 can be factory-programmed to any frequency between 1 and 60 MHz. This programmability enables designers to optimize clock configuration while eliminating the long lead time and customization cost associated with quartz based OCXOs of which each frequency is custom built.

Features

- Any frequency between 1 and 60 MHz, in 1Hz steps
- ±0.3 ppb/°C frequency slope (ΔF/ΔT)
- ±5 ppb over-temperature stabilities. Contact SiTime for ±2 and ±3 ppb options
- Up to 85°C operating temperature ranges, contact SiTime for 105°C option
- 3e-11 ADEV at 1 second average time
- Exceptional dynamic stability under airflow and rapid temperature changes
- Excellent Holdover over a wide range of conditions
- Integrated regulators for on-chip power-supply noise filtering and excellent PSRR
- GR-1244 Stratum 3E compliant
- Resistant to shock, vibration and board bending
- 3.3V supply voltage (contact SiTime for other voltages)
- Contact SiTime for I^2C Voltage Control options
- LVCMOS output, Contact SiTime for Clipped Sinewave
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Applications

- 4G/5G radio
- Base Stations
- Digital Switching
- Time and Frequency Measurement
- IEEE1588
- Test and measurement

9.0 x 7.0 mm Package

Figure 1. Top and bottom view

Package Pinout

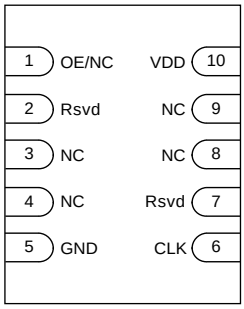


Figure 2. Pin Assignments (Top view)

Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3V VDD.

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Output Frequency Range	F	1	–	60	MHz	
Frequency Stability						
Frequency Stability over Temperature	F_stab	-5	–	+5	ppb	Referenced to (fmax + fmin)/2 over the specified temperature range
		-8	–	+8	ppb	
Frequency vs. Temperature Slope	ΔF/ΔT	–	±0.3	–	ppb/°C	In still air, 1°C/min ramp rate
Dynamic Frequency Change to Temperature Ramp	F_dynamic	–	±0.005	–	ppb/s	In still air, 1°C/min ramp rate
Initial Tolerance	F_init	–	±500	–	ppb	Initial frequency at 25°C inclusive of solder-down shift at 48 hours after 2 reflows
24-hour drift	F_24_Drift	–	±0.9	–	ppb	Measured at 25°C after 30 days continuous operation
Hysteresis Over Temperature	F_Hys	–	–	+1	ppb	Over -20 to 70 °C, measured as max frequency spread of hysteresis eye
		–	–	+1.6	ppb	Over -40 to 85 °C, measured as max frequency spread of hysteresis eye
One-Day Aging	F_1d	–	±0.8	–	ppb	After 30-days operation
One-Month Aging	F_1m	–	±25	–	ppb	After 30-days operation
One-Year Aging	F_1y	–	±150	–	ppb	After 30-days operation
20-Year Aging	F_20y	–	±500	–	ppb	After 30-days operation
Total Stability – 20 years	F_20y_stab	-4.6	–	+4.6	ppm	Stratum 3E per GR-1244 Core. Inclusive of initial tolerance, frequency stability over temperature, 20-year aging, and variations to supply voltage and output load. Typically called free running accuracy
Supply Voltage Sensitivity	F_vdd	–	±1	–	ppb	Vdd ±5%
Output Load Sensitivity	F_load	–	±1	–	ppb	LVCMOS output, 15 pF ±10%
		–	±1	–	ppb	Clipped sinewave output, 10kΩ, 10 pF ±10%
Start-up Characteristics						
Start-up Time	T_start	–	5	–	ms	Time to first pulse
Time to Rated Stability	T_stability	–	2	–	min	Time to first accurate pulse within rated stability
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	tr, tf		1		ns	10% - 90% VDD
Output Voltage High	V_{OH}	90%			V_{DD}	I_{OH} = -6 mA, (Vdd = 3.3V)
Output Voltage Low	V_{OL}			10%	V_{DD}	I_{OL} = 6 mA, (Vdd = 3.3V)
Clipped Sinewave Output Characteristics						
Output Voltage Level	V_{OUT}	0.8	–	1.2	V	Measured peak-to-peak swing at any Vdd – 10kΩ || 10 pF ±10%
Rise/Fall Time	tr, tf		1		ns	10% - 90% V_{DD}

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	V_{DD}	3.14	3.3	3.47	V	Contact SiTime for other voltage options
Power Consumption						
Power Consumption – Warm up	Pwr_warmup		2.5		W	Max power may be configurable lower, higher max gives shorter time.
Power Consumption – Steady State	Pwr_steady		0.60		W	At +50°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial
		-40	–	+85	°C	Industrial. Contact SiTime for 105°C support

Table 3. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	–	30	–	kΩ	Internal pull up to VDD
Input High Voltage	VIH	70	–	–	%	
Input Low Voltage	VIL	–	–	30	%	

Table 4. Jitter & Phase Noise

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Period Jitter	T_jitt	–	0.8	–	ps	F = 10 MHz, population 10k
RMS Phase Jitter (random)	T_phj	–	0.31	–	ps	F = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	–	ps	F = 50 MHz, Integration bandwidth = 12 kHz to 20 MHz
Peak Cycle-to-Cycle Jitter	T_jitt_cc	–	6	–	ps	F = 10 MHz, population 1k, measured as absolute value
Allan Deviation						
$\tau = 1\ second$	AD_1s	–	3 E-11	–		
$\tau = 10\ seconds$	AD_10s	–	2 E-11	–		
$\tau = 100\ seconds$	AD_100s	–	2 E-11	–		
Phase Noise						
1 Hz offset		–	-80	–	dBc/Hz	Reference f = 10 MHz
10 Hz offset		–	-108	–	dBc/Hz	
100 Hz offset		–	-127	–	dBc/Hz	
1 kHz offset		–	-148	–	dBc/Hz	
10 kHz offset		–	-154	–	dBc/Hz	
100 kHz offset		–	-154	–	dBc/Hz	
1 MHz offset		–	-167	–	dBc/Hz	
5 MHz offset		–	-168	–	dBc/Hz	

Table 5. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb-free soldering guidelines)	–	260	°C

Table 6. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method2002**
Mechanical Vibration	**MIL-STD-883F, Method2007**
Temperature Cycle	**JESD22, MethodA104**
Solderability	**MIL-STD-883F, Method2003**
Moisture Sensitivity Level	**TBD**

Pin-outs

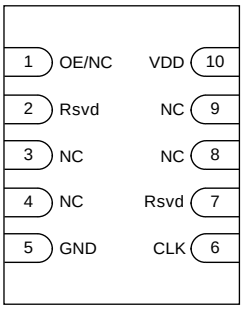


Figure 3. Pin Assignments (Top view)

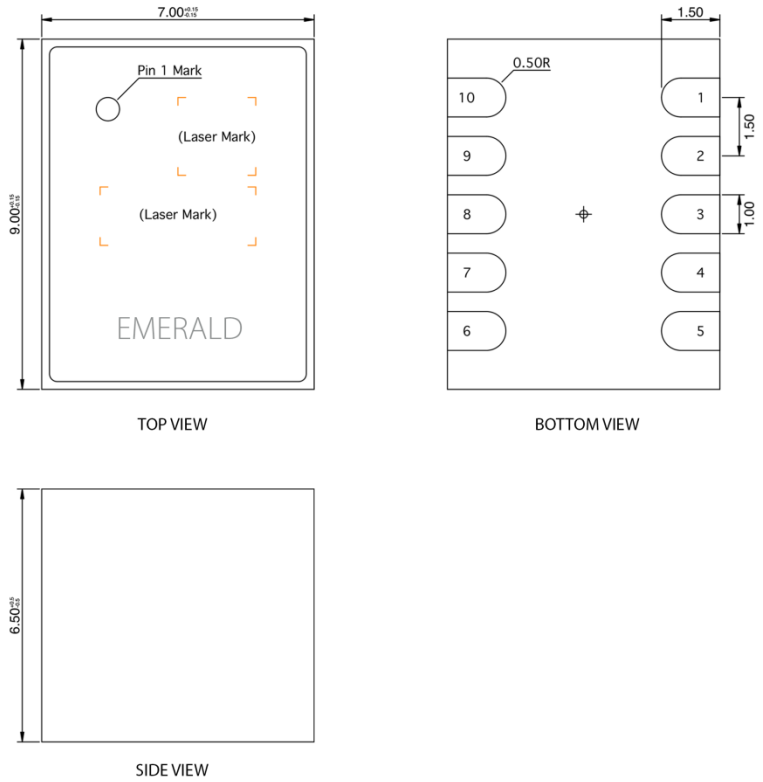
Table 7. Pin Description

Pin	Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
1	OE/NC	OE – Input	100 kΩ Pull-Up	H[1]: specified frequency output L: output is high impedance. Only output driver is disabled
		NC – No Connect	-	H or L or Open: No effect on output frequency or other device functions
2	Rsvd	Reserved	-	Connect to VDD or leave it open
3	NC	No Connect	-	H or L or Open: No effect on output frequency or other device functions
4	NC	No Connect	-	H or L or Open: No effect on output frequency or other device functions
5	GND	Power	-	Connect to ground[2]
6	CLK	Output	-	LVCMOS, or clipped sinewave oscillator output
7	Rsvd	Reserved	-	Connect to VDD or leave it open
8	NC	No Connect	-	H or L or Open: No effect on output frequency or other device functions
9	NC	No Connect	-	H or L or Open: No effect on output frequency or other device functions
10	VDD	Power	-	Connect to VDD

Notes:
1. In OE mode, a pull-up resistor of 100 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
2. 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND.

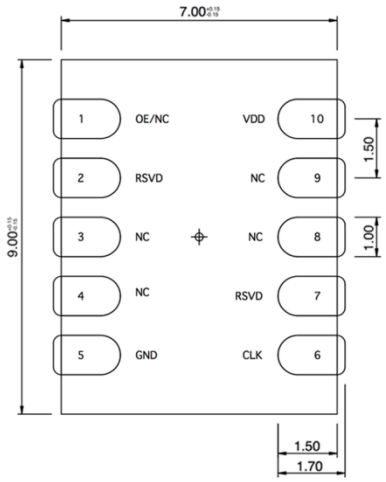
Dimensions and Patterns (9 mm x 7 mm package)

Package Size – Dimensions (Unit: mm)



Package Outline	
Emerald V.4 Footprint	SiTime Confidential
Scale: 1cm=1mm	SiTime
AP 2018/08/23	

Recommended Land Pattern (Unit: mm)



Solder Print Layout	
Emerald V.4 Footprint	SiTime Confidential
Scale: 1cm=1mm	SiTime
AP 2018/08/08	

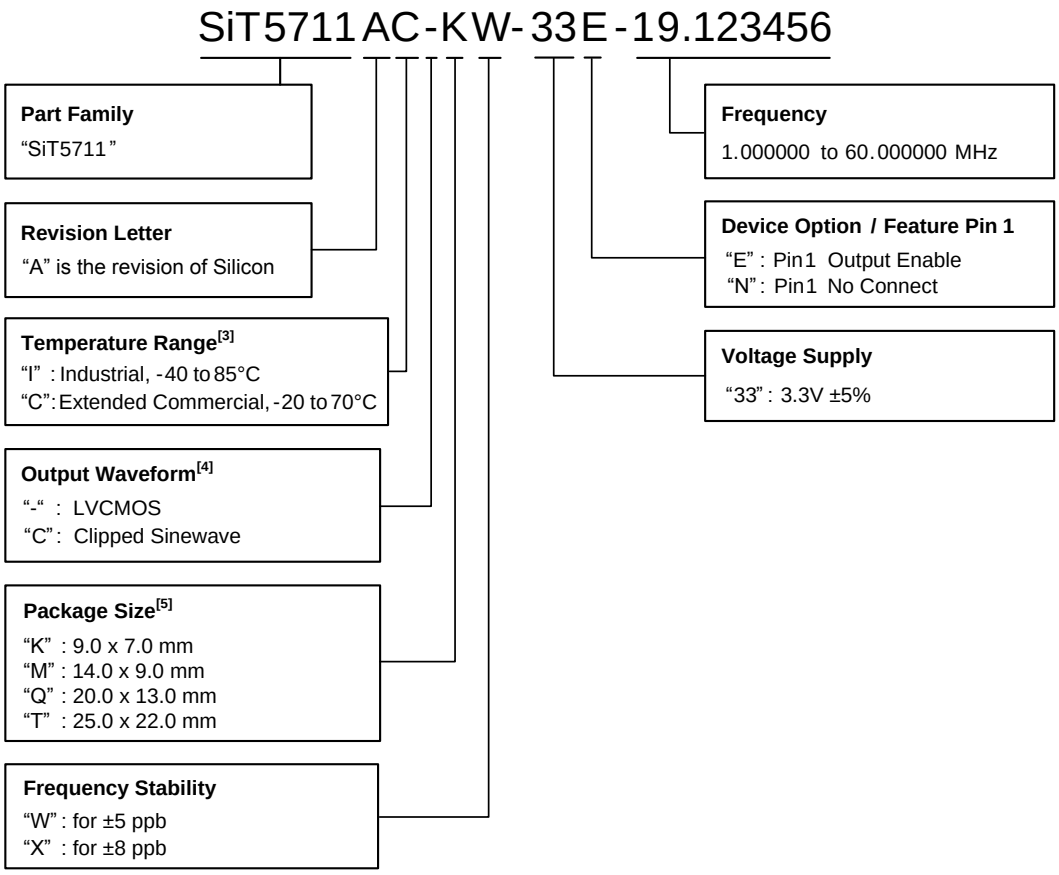
Layout Guidelines

- SiT5711 uses internal regulators to minimize the impact of the power supply noise. For further reduction of noise, it is essential to use two bypass capacitors (0.1 µF and 10 µF). Place the bypass capacitors as close to the VDD as possible, typically within 1 to 2 mm. Ensure 0.1uF cap the closest to the device VDD and GND power pins.
- It is also recommended to connect all NC pins to the ground plan and place multiple vias under GND pin for maximum heat dissipation.
- For additional layout recommendations, refer to the Best Design Layout Practices.

Manufacturing Guidelines

- No Ultrasonic or Megasonic Cleaning: Do not subject the SiT5711 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- No metal cover. Unlike legacy quartz OCXO, SiT5711 is engineered to operate reliably without performance degradation, in the presence of ambient disturbers such as airflow and sudden temperature changes. Therefore, the use of a metal cover typical of quartz OCXO is not needed.
- Reflow profile, per JESD22-A113D.
- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

Ordering Information



Notes:

3. Contact SiTime for higher temperature range options
4. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI.
5. Contact SiTime for 14.0 x 9.0 mm, 20.0 x 13.0 mm, 25.0 x 22.0 mm footprints.